Transconductance and slew rate improvement technique for current recycling folded cascode amplifier

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**Abstract**

A proposed technique to achieve transconductance and slew rate improvement of current recycling folded cascode amplifier is presented in this paper. It adopts the local common-mode feedback structure to increase gain-bandwidth, dc gain and slew rate of conventional recycling current amplifiers with no additional power dissipation. A proposed amplifier based on this technique is simulated on UMC 180 nm process. The simulation results demonstrate that the proposed amplifier achieves a 200\% gain-bandwidth, 10 dB dc gain and 100\% slew rate improvement with the same power dissipation when compared to the conventional current recycling counterparts.

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1. Introduction

In switched-capacitor (SC) circuits, the operational transconductance amplifiers (OTAs) are critical analog blocks, which require fast settling response and precise final value [1]. Therefore, the high performance OTAs should have high dc gain, wide gain-bandwidth (GBW) and large slew rate [2]. In recent years, the current recycling folded cascode OTAs (RFC) get preferred over conventional folded cascode OTAs (FC), owing to the improved GBW, dc gain and slew rate [3,4]. Some techniques to further improve the effective transconductance and slew rate of RFC are also presented, such as current–shunt technique, positive-feedback technique and double-recycling technique [5–7]. In [5], current–shunt technique is employed in the cross-coupled current mirrors to separate dc and ac path of recycling structure, leading to a significant boost in GBW and slew rate. In [6], positive-feedback technique is utilized to form the positive-feedback current mirror loads to improve the gain of recycling structure, achieving the enhancement of general performance compared to RFC. And in [7], an increased recycling path is used to double recycling the input signal, improving the GBW and slew rate of RFC with no additional power. Although the presented techniques have improved the GBW and slew rate of RFC, all of them lower the location of first non-dominant poles, and thus degrade the phase margin, causing stability issues of OTAs.

In this paper, a proposed technique to achieve the enhancement of general performance, including the GBW, slew rate and dc gain, of the conventional RFC is presented. It is based on the local common-mode feedback structure, not only improving the effective transconductance and dc gain, but also boosting the slew rate [8–10]. Most of all, the enhanced performances introduced by this proposed technique are at no cost of power penalty and preserving stability.

This paper is organized as follows. The conventional RFC is discussed in Section 2. In Section 3, the amplifier based on the proposed technique to improve the transconductance and slew rate is described and the circuit performances including GBW, dc gain, slew rate, stability and noise performance are discussed. To demonstrate the enhanced performances of proposed technique, two OTAs are designed and compared in Section 4. And the conclusions are given in Section 5.

2. The conventional RFC amplifier

The conventional RFC is shown in Fig. 1 [3,4] where all transistors operate in the saturation region. The input differential pairs is split to M1a and M1b. Transistor M1b is used to recycle input signal current, which is then amplified by a factor of \(K\) through cross-over mirror current M3:M2. Thus, the equivalent transconductance (\(G_m\)) of RFC is given as [3,4],

\[
G_{mRFC} = (K + 1)G_{m1a}
\]

(1)
consequently the GBW of the RFC is \[3,4],
\[
GBW_{RFC} = \frac{(K + 1)g_{m1a}}{C_l}
\]  
(2)
where \(C_l\) is the load capacitance. Owing to the enhanced transconduction, its dc gain is also improved. Meanwhile, the slew rate (SR) of RFC is also given as \[3,4],
\[
SR_{RFC} = \frac{2K\beta_2}{C_l}
\]  
(3)
where \(2\beta_2\) is the bias current of input pairs. Therefore, in order to obtain a higher slew rate and GBW, the enhancement factor \(K\) must be larger. However, an increase in \(K\) leads to not only the same increase in power consumption, but also larger parasitic capacitances at node X, reducing the phase margin. The non-dominant pole at node X can be described as \[4\]
\[
\omega_X = \frac{g_{m2}}{(K + 1)C_{gs2}}
\]  
(4)
where \(C_{gs2}\) is the gate-to-source capacitance of transistor M2. Thus, the value of \(K\) should not be too large, and a reasonable value is set to 3. For this reason, the GBW and SR of RFC is twice and three times that of conventional FC counterpart with the same power dissipation.

3. The proposed CFRFC amplifier

The proposed OTA based on the local common-mode feedback structure (CFRFC) is shown in Fig. 2 where all transistors operate in the saturation region. The active current mirror load of input pairs M1b are substituted by the local feedback loops composed by matched resistors R1. The common-mode drain voltages of transistor M2 are fed back to their gate terminal. In quiescent conditions, no current flows through resistors R1, and voltage at node X, Y equals that at node Z, which can be given as,
\[
V_X = V_Y = V_Z = V_{THN} + \sqrt{\frac{I_B}{\beta_2}}
\]  
(5)
where \(V_{THN}\) and \(\beta_2\) are the threshold voltage of NMOS transistor and transconductance factor of M2. Thus, the ratio of quiescent current \(I_q\) through M2 and M3 is set by their \(W/L\) size ratio,
\[
\frac{I_{0,M3}}{I_{0,M2}} = \frac{(W/L)_{M3}}{(W/L)_{M2}}
\]  
(6)
Note that if this ratio factor is chosen to be \(K\), the power consumption is the same as that of RFC.

3.1. Transconductance and GBW improvement

For small signal analysis of the proposed CFRFC OTA, ac current would go through R1 and node Z becomes virtual ground. Thus, the expressions for equivalent transconductance \((g_{m2})\) can be given as
\[
G_mCFRFC \equiv \left(1 + g_{m3} r_{ds1}\right) g_{m1a} \equiv (1 + g_{m3} R_1) g_{m1a}
\]  
(7)
where \(r_{ds}\) is drain–source resistance of transistors. With a large value of \(R_1\), \(g_{m3} R_1\) would be larger than \(K\), which leads to a significant boost in transconductance compared to the conventional RFC at the same quiescent power conditions. Also, the GBW of the proposed CFRFC are expressed as follows,
\[
GBW \equiv \left(1 + g_{m3} R_1\right) g_{m1a} C_l
\]  
(8)
where \(C_l\) represent the load capacitance at the output node. Note that due to increased transconductance, the enhancement of GBW is also obtained.

3.2. DC gain enhancement

The output equivalent resistance \((R_{out})\) of the proposed CFRFC can be given as follows,
\[
R_{out} \equiv \left[\left(g_{m5} r_{ds5}\right) r_{ds6} \right] \left[\left(g_{m4} r_{ds4}\right) r_{ds3} \right] r_{ds1}\]
\]  
(9)
Note that the output impedance of CFRFC is the same as that of RFC counterpart. And then the dc open-loop gain can be described as,
\[
A_{dc} \equiv \left(1 + g_{m3} R_1\right) g_{m1a} R_{out}
\]  
(10)
It is noticed that due to the improved transconductance, the dc gain of the proposed CFRFC is accordingly enhanced.

3.3. Slew rate boost

The large signal response of CFRFC can be analyzed as follows. Assume that a large positive step applied to \(V_{in}\), the input differential pairs M1a and M1b in left side will be cut off, and then voltage at node Y decreases, forcing transistors M2, M3 and M4 in the right side turn off. Due to transistor M3 in the right side is cut off, the input transistor M1a in the right side goes into triode region. The tail current 2\(I_B\) enters into M1b in the right side. Because of the local common–mode feedback, half of tail current flow through R1, and the other half goes into M2. Therefore, the maximum voltage swing

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**Fig. 1.** The conventional RFC amplifier.

**Fig. 2.** The proposed CFRFC amplifier.
at node X(Y) is IbR1. Meanwhile, with the help of M3, the maximum current delivered to the load CL will be approximately

\[ I_{\text{max}}^\text{out} \simeq \beta_3 (V_{Q,X} + IbR_1)^2 \]  

(11)

where \( V_{Q,X} \) is the quiescent voltage at node X. It is noticed that if a large value of \( R_1 \) is chosen, the large dynamic currents are generated, Owing to square relationship between the output current and voltage swing at node X(Y), the maximum output current would be much higher than that of RFC counterpart.

The slew rate of the proposed CFRFC is therefore expressed as

\[ S_{\text{RFC}} \simeq \frac{I_{\text{max}}^\text{out}}{C_L} \]

(12)

Note that when slewing behavior happens, the slew rate of the proposed CFRFC is significantly enhanced than that of RFC with the same quiescent current. Table 1 summarizes the performance metrics for both configurations.

### 3.4. Influence of resistance mismatch

The mismatch of resistance R1 has some influences on the performance metrics of CFRFC OTAs. Assume that the value of two resistances are \( R + \Delta R \) and \( R \), when ac current goes through them, the differential equivalent resistance is \( R + \Delta R/2 \) and \( R - \Delta R/2 \). Therefore, the variation of equivalent transconductance (\( \Delta G_m \)) can be given as,

\[ \Delta G_m^{\text{RFC}} \equiv \left( \frac{g_m 3 \Delta R}{2} \right) g_{m1a} \]

(13)

So as the variations of GBW (\( \Delta \text{GBW} \)) and dc gain (\( \Delta A_{dc} \)) can be, respectively, expressed as

\[ \Delta \text{GBW} \equiv \left( \frac{g_m 3 \Delta R}{2} \right) g_{m1a} \]

(14)

\[ \Delta A_{dc} \equiv \left( \frac{g_m 3 \Delta R}{2} \right) g_{m1a} R_{\text{out}} \]

(15)

As for the large signal performance, the variation of slew rate (\( \Delta S_R \)) can be described as,

\[ \Delta S_{\text{RFC}} \equiv \frac{S_{\text{RFC}}^\text{max}}{C_L} \Delta G_m^{\text{RFC}} \]

\[ \approx \frac{\beta_3 (I_b \Delta R/2)^2}{C_L} + \frac{\beta_3 (-I_b \Delta R/2)^2}{C_L} \]

(16)

Note that the mismatch of resistance \( R_1 \) would degrade the performance metrics of CFRFC, causing variation of GBW, dc gain and slew rate. And thus the layout of resistances \( R_1 \) should be carefully considered to reduce the mismatch.

### 3.5. Stability performance

The phase margin is an important consideration of amplifiers. The transfer function of the proposed CFRFC has thee poles. The dominant pole \( p_1 \) locates at output node, which is approximately

\[ p_1 \approx \frac{1}{R_{\text{out}}L} \]

(17)

The first non-dominant pole \( p_2 \) caused by the local common-mode feedback structure locates at node X(Y), and it is approximately

\[ p_2 \approx \frac{1}{(R_1 + R_2 + R_3)(C_{gs3} + C_{db2} + C_{db10})} \approx \frac{1}{R_1C_{gs3}} \]

(18)

Also the second non-dominant pole \( p_3 \) locates at the source terminal of transistors M4, which can be expressed as

\[ p_3 \approx \frac{g_m 3}{C_{gs4} + C_{db3} + C_{db1a}} \]

(19)

In order to maintain stability of amplifier, \( p_2 > 3 \text{GBW} \) should be satisfied. Thus, the upper boundary on \( R_1 \) can be described by

\[ (1 + g_m 3 R_1) < \frac{C_L}{3g_m 1 C_{gs3}} \]

(20)

Note that in spite of a large value of \( R_1 \) would improve the GBW, dc gain and slew rate, too large \( R_1 \) will lower the non-dominant pole, degrading the phase margin of the proposed CFRFC. Therefore, a reasonable value of \( R_1 \) should be carefully chosen.

### 3.6. Noise performance

The noise performance is another important consideration for design. The power spectral density of the thermal noise current of MOS transistors is given by

\[ i_0^2 = 4kTg_m \]

(21)

where k is Boltzmann constant, \( T \) is absolute temperature, \( \gamma \) is coefficient derived to be equal to 2/3 for long-channel transistors and \( g_m \) is transconductance of transistors.

For conventional RFC, the input referred thermal noise can be expressed as,

\[ i_{\text{rf,RFC}}^2 = \frac{8kT\gamma}{g_m 1(1 + K)^2} \cdot [g_m 1a(1 + K^2) + g_m 3(1 + K) + g_m 5] \]

(22)

while for the proposed CFRFC, the input referred thermal noise can be given as,

\[ i_{\text{rf,CFRFC}}^2 = \frac{8kT\gamma}{g_m 1a(1 + K + g_m 3 R_1)} \cdot [g_m 1a(1 + g_m 3 R_1^2) + g_m 3(1 + g_m 3 R_1^2/K + g_m 1 R_1/\gamma) + g_m 5] \]

(23)

Note that the resistances \( R_1 \) contribute noises to the output node, causing the increased total noises of CFRFC. Fortunately, owing to the significant enhanced transconductance, the input referred noise of CFRFC would not be worsen when compared to RFC counterparts.

### 4. Simulation results and discussion

To demonstrate the enhanced performance by the proposed technique, two OTAs (conventional RFC and proposed CFRFC) are designed and simulated on UMC 180 nm process. The supply voltage is 1.0 V, and \( I_b \) is set to 10 \( \mu \)A. The load capacitance \( C_L \) is 30.0 pF, and it is realized by MOS capacitors to reduce area penalty. Both OTAs has the same quiescent bias current and transistor size. Resistors \( R_1 \) have value of 50 k\( \Omega \), and it is implemented using polysilicon strips. Also, if linearity is not critical, they can be realized by MOS transistors in triode region to save active area. The size ratio of main transistors for two OTAs are shown in Table 2. The performance metrics is obtained under Cadence Spectre simulation tools and the MOS model is used the BSIM3v3 models.

Fig. 3 shows the simulated open-loop AC response of RFC and CFRFC OTAs. It is noticed that the GBW of the proposed CFRFC achieves 10.2 MHz, while conventional RFC is only 3.1 MHz. Due to the enhanced transconductance of proposed technique, the GBW of
CFRFC improves 230% over that of RFC with the same power consumption. Also, it can be seen that the dc gain of CFRFC is 10 dB higher than that of RFC, also attributing to the improved transconductance. In spite of there is slightly degradation compared with RFC, the phase margin of CFRFC still maintain above 80°. Thus, the enhanced GBW and dc gain of CFRFC are at no expense of stability.

To discuss influence of process mismatches and spreads, including mismatch parameters for resistance, the Monte Carlo analysis over 1000 runs are simulated. The results regarding ac response of RFC and CFRFC are shown in Table 3. It is noticed that even under mismatch conditions, the GBW of CFRFC still improves at least 200% over that of RFC. Also, dc gain of CFRFC is almost 10 dB higher than that of RFC. And the phase margin of CFRFC maintains at the level of 80°.

Fig. 4 shows the small signal transient response of RFC and CFRFC OTAs. A square wave of 100 mV at 500 kHz is generated, and both OTAs are configured as voltage follower. For the RFC and CFRFC, the 1% settling times are 405 and 136 ns, respectively. Note that the settling time of CFRFC enhances three times of that of RFC, which corresponds to the improvement of GBW of two OTAs. Also, no ringing happens in either step response, which demonstrates the phase margin of CFRFC has almost no degradation in spite of improved GBW and settling time.

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Fig. 5 shows that the large signal transient response of RFC and CFRFC. A large step wave of 400 mVpp at 500 kHz are applied. For the RFC and CFRFC, the average slew rates are 0.88 and 1.78 V/μs, respectively. It is noticed that the slew rate of CFRFC is almost two times that of RFC with the same quiescent current, which attributes to the enhanced maximum dynamic output current caused by the local common-mode feedback structure. Also, there is no ringing in either step response, which shows the local common-mode feedback has negligible influence on the phase margin.

The spectral density of input referred thermal noise of RFC and CFRFC is shown in Fig. 6. For the RFC and CFRFC, the simulated input referred thermal noise are 26 and 22 nV/√Hz, respectively. Although additional resistance R1 contributes more noise than that of RFC, the significant improved transconductance decrease the effect of R1, as described in Eqs. (22) and (23). Thus, the noise performance of CFRFC will not be worse than that of RFC.

The simulation results of key parameters of RFC and CFRFC are listed in Table 4. It can be seen that the CFRFC based on the proposed technique in this paper achieves three times improved GBW, 10 dB higher dc gain and twice enhanced slew rate that of RFC at the same power dissipation.

In order to evaluate the proposed technique in this paper, the CFRFC is compared to other current recycling OTAs, including the current-shunt, positive-feedback and double-recycling OTAs presented in previous papers. Due to these OTAs are designed and

### Table 2

<table>
<thead>
<tr>
<th>Transistors (μm/μm)</th>
<th>RFC OTAs</th>
<th>CFRFC OTAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1(a/b)</td>
<td>60/0.36</td>
<td>60/0.36</td>
</tr>
<tr>
<td>M2</td>
<td>12/0.5</td>
<td>12/0.5</td>
</tr>
<tr>
<td>M3</td>
<td>36/0.5</td>
<td>36/0.5</td>
</tr>
<tr>
<td>M4</td>
<td>6/0.18</td>
<td>6/0.18</td>
</tr>
<tr>
<td>M5</td>
<td>15/0.18</td>
<td>15/0.18</td>
</tr>
<tr>
<td>M6</td>
<td>24/0.5</td>
<td>24/0.5</td>
</tr>
<tr>
<td>M7</td>
<td>48/0.5</td>
<td>48/0.5</td>
</tr>
<tr>
<td>M8</td>
<td>3/0.18</td>
<td>-</td>
</tr>
<tr>
<td>R1</td>
<td>-</td>
<td>50 k</td>
</tr>
</tbody>
</table>

### Table 3

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RFC OTAs</th>
<th>CFRFC OTAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain average (dB)</td>
<td>68.7</td>
<td>78.3</td>
</tr>
<tr>
<td>DC gain standard deviation (dB)</td>
<td>1.37</td>
<td>1.69</td>
</tr>
<tr>
<td>GBW average (MHz)</td>
<td>3.14</td>
<td>9.67</td>
</tr>
<tr>
<td>GBW standard deviation (MHz)</td>
<td>0.61</td>
<td>0.81</td>
</tr>
<tr>
<td>Phase-margin average (°)</td>
<td>83.4</td>
<td>78.2</td>
</tr>
<tr>
<td>Phase-margin standard deviation (°)</td>
<td>2.6</td>
<td>4.1</td>
</tr>
</tbody>
</table>

![Fig. 3. The simulated open-loop AC response of the two OTAs.](image)

![Fig. 4. The small signal transient response of the two OTAs.](image)

![Fig. 5. The big signal transient response of the two OTAs.](image)
simulated under different processes, supply voltage, bias current and load capacitance, the FoM value is employed here, which can be shown as follows

\[ \text{FoM}_1 = \frac{\text{GBW} \times C_L}{I_{\text{Qtotal}}} \]  

where \( I_{\text{Qtotal}} \) is total quiescent current of OTAs. The comparison results are listed in Table 5.

Note that the conventional RFC has the least energy efficiency, and the current-shunt [5], positive-feedback [6] and double-recycling OTAs [7] improve the energy efficiency when compared to the RFC. However, all these present techniques not significantly enhance the large signal performance of RFC. Therefore, the proposed CFRFC significantly improves not only the small signal current efficiency, but also the large signal current efficiency compared to other recycling OTAs, which demonstrates the enhanced performance introduced by the proposed technique in this paper.

5. Conclusion

A proposed technique to enhance the GBW, slew rate and dc gain of the conventional RFC is presented in this paper. Based on the local common-mode feedback structure, the proposed CFRFC OTA improves 200% GBW, 10 dB dc gain and 100% slew rate with the same power dissipation compared to conventional recycling counterparts.

Acknowledgements

This work is supported by the Fundamental Research Funds for the Central Universities of China (No. 2652014070), the National Natural Science Foundation of China (No. 41204135) and the National “863” Program of China (No. 2012AA061102).

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