Transconductance improvement method for low-voltage bulk-driven input stage

Xiao Zhao\textsuperscript{a,b}, Huajun Fang\textsuperscript{c,*}, Tong Ling\textsuperscript{c}, Jun Xu\textsuperscript{c}

\textsuperscript{a} Key Laboratory of Geo-detection (China University of Geosciences, Beijing), Ministry of Education, PR China
\textsuperscript{b} School of Geophysics and Information Technology, China University of Geosciences (Beijing), Beijing 100083, PR China
\textsuperscript{c} Institute of Microelectronics, Tsinghua University, Beijing 100084, PR China

\section{1. Introduction}

With the development of portable and biomedical applications, low-voltage and low-power analog and mixed signal ICs are required in increasing demands\cite{1,2,3}. One of the main analog building blocks is the operational transconductance amplifier (OTA), which is the largest and most power consuming\cite{4,5}. To reduce the power dissipation and supply voltage, CMOS circuits working in weak inversion region are good choices since they have high $g_{m}/I$ ratio, providing high energy efficiency\cite{6,7}. In addition, to operate in a wide voltage range in low-voltage condition, bulk-driven circuits are typically used to overcome issues of the reduction of input voltage range\cite{8,9,10,11}.

However, the main problem associated with the bulk-driven technique in the weak-inversion region is that the bulk transconductance ($g_{mb}$) is substantially smaller than that in the strong inversion region. This insufficient transconductance will affect the performance of the OTA, such as unity-gain bandwidth (GBW), open-loop gain, and input-referred noise\cite{12,13,14}.

In recent years, many methods to increase the effective transconductance of the bulk-driven input stage were developed\cite{15,16,17,18,19,20,21,22,23}. The bulk-driven input stage utilizing partial positive feedback technique has been adopted by several recent works\cite{16,17,19,23}. However, due to device mismatches and process variations, the positive-feedback loop gain that is too close to unity could cause serious stability issues inside the input stage\cite{24}.

In this paper, a proposed bulk-driven input stage with current–shunt auxiliary pairs to significantly enhance transconductance is presented. The basic idea is to use current–shunt auxiliary differential pairs to improve the voltage gain from the inputs to the gates of the bulk-driven pairs. The enhanced transconductance leads to the improvement of gain bandwidth and dc gain of the OTA with a higher figure-of-merit (FoM).

This brief is organized as follows. In Section 2, we will describe the bulk-driven input stage with conventional transconductance method, and then introduce the proposed bulk-driven input stage with current–shunt auxiliary pair and the detailed circuit analysis. The circuit performance and comparison is next presented in Section 3, with conclusions given in Section 4.

\section{2. The proposed transconductance enhanced bulk-driven OTA}

\subsection{2.1. The bulk-driven input stage in weak inversion}

The drain current $I_{DS}$ of a MOS transistor operating in weak inversion can be given by

\begin{equation}
I_{DS} = I_{S} \left( \frac{W}{L} \right) \exp \left( \frac{V_{CS} - V_{TH}}{n k T} \right) \left[ 1 - \exp \left( - \frac{V_{DS}}{k T} \right) \right]
\end{equation}

Please cite this article as: X. Zhao, et al., Transconductance improvement method for low-voltage bulk-driven input stage, INTEGRATION, the VLSI journal (2014), http://dx.doi.org/10.1016/j.vlsi.2014.11.005
where \( I_B \) is the characteristic current and \( n \) is the slope factor in weak inversion [25]. In weak inversion region, if \( V_{DS} > 3kT/q \), the transistor will be saturated. In weak inversion region, the transconductance \( g_m \) can be presented in (2), which is a function of current \( I_{DS} \) only.

\[
g_m = q \frac{I_{DS}}{nkT} \tag{2}
\]

However, in the bulk-driven differential pairs, which is shown in Fig. 1, the most significant issue is its small bulk transconductance \( g_{mb} \) compared to the gate transconductance \( g_m \). The ratio \( \eta \) of \( g_{mb} \) to \( g_m \) is expressed as

\[
\eta = \frac{g_{mb}}{g_m} = \frac{2}{\sqrt{2}n + V_{BS}} \tag{3}
\]

Normally, the ratio \( \eta \) only ranges from 0.2 to 0.4 depending on the bulk-to-source voltage \( V_{BS} \) and other specific process parameters. Thus, the effective transconductance \( G_{meff} \) of the bulk-driven OTA working in weak-inversion region is reduced significantly.

### 2.2. The conventional bulk transconductance double-enhanced input stage

In the bulk-driven input stage, as shown in Fig. 1, the input signal is applied to the bulk terminal of the input pairs to modulate the drain-to-source current \( I_{DS} \), thus the input common-mode voltage range of the circuit is extended to the rail-to-rail operation [26,27]. However, the gate terminal of the bulk-driven input transistors is left unexplored, which is only biased at a constant voltage to turn on the transistors, to conduct a small signal current.

In the conventional bulk transconductance double-enhanced technique, shown in Fig. 2, cross-connected bulk-driven transistors \( M3 \) and \( M4 \) form one auxiliary differential pair to modulate the gate of the input pairs \( M1 \) and \( M2 \) [24]. Thus, both the bulk and the gate terminals of bulk-driven transistors \( M1 \) and \( M2 \) in this configuration are modulated directly or indirectly by the input signals.

Small signal equivalent circuit of this bulk-driven input stage in Fig. 2 is analyzed and the effective transconductance \( G_{meff} \) can be expressed by

\[
G_{meff} = \frac{g_{mb4}}{g_{m4}} \times g_{m1} + \frac{g_{mb1}}{g_{mb} \times g_{m1}} + \frac{1}{\eta \times g_{m4}} \times g_{m1} + \frac{1}{\eta \times g_{mb1}} = 2 \times g_{mb1} \tag{4}
\]

where \( g_{mb4} \) and \( g_{mb1} \) are the bulk transconductances of the transistors \( M4 \) and \( M1 \), and \( g_{m4} \) and \( g_{mb} \) is the transconductance of \( M4 \). Note that regardless of the \( g_m \) or \( g_{mb} \) of the auxiliary differential pairs \( M3 \) and \( M4 \), the effective transconductance of the bulk-driven input stage is doubled. However, as dc and ac currents share the same path, the boost of effective transconductance is limited by the factor of 2 [24].

### 2.3. The proposed bulk transconductance double-enhanced input stage

To further improve the effective transconductance, an enhanced bulk-driven input stage utilizing current-shunt auxiliary pair, shown in Fig. 3, is presented in this section. The basic idea is to use current-shunt auxiliary differential pairs to improve the voltage gain from the inputs to the gates of the bulk-driven input transistors \( M1 \) and \( M2 \).

In the proposed structure, as shown in Fig. 3, NMOS transistors \( M5 \) and \( M6 \) are diode-connected, while \( M7 \) and \( M8 \) act as current sinks to shunt partial bias current \((1 - 1/N)I_{B}, N > 1\) to the ground. Thus, dc and ac currents of the proposed auxiliary differential pair have different paths. DC currents flow through \( M7 \) and \( M8 \), while almost no ac current flows through \( M7 \) and \( M8 \) since they show high impedance for ac signals. The separated dc and ac paths increase the impedance at the node \( A \) without extra current consumption, so that the voltage gain of the auxiliary differential pair is further improved.

Since the transconductance in the weak-inversion region is proportional to the bias current \( I_B \) flowing through transistors, the \( g_m \) of \( M5 \) and \( M6 \) is \( 1/N \) times that of \( M3 \) and \( M4 \). Then the effective transconductance \( G_{meff} \) of the proposed bulk-driven input stage including these auxiliary differential pairs can be given as

\[
G_{meff} = \frac{g_{mb4}}{g_{m4}} \times g_{m1} + \frac{g_{mb1}}{g_{mb} \times g_{m1}} + \frac{1}{\eta \times g_{m4}} \times g_{m1} + \frac{1}{\eta \times g_{mb1}} = \frac{N + 1}{N} \times g_{mb1} \tag{5}
\]

As a consequence, with proper value of \( N \), the effective transconductance is significantly improved by a factor of \( N \) compared...
to the conventional counterpart. Clearly, the overall input stage transconductance of the proposed input stage does not depend on the absolute $g_m$ or $g_{mh}$ values of the auxiliary differential pairs M3 and M4. Thus, from power consumption standpoint, downsizing the ratios of transistors and the bias current of auxiliary pair will improve the input stage efficiency.

Nevertheless, in frequency domain, one pole and zero doublet associated with the node A is introduced by the proposed auxiliary differential pair and they can be expressed as

$$z_A = \frac{2 \cdot g_{m5}}{N \cdot C_A} - \frac{2 \cdot g_{m3}}{N \cdot C_A}$$

(6)

$$p_A = \frac{g_{m5}}{C_A} - \frac{g_{m3}}{N \cdot C_A}$$

(7)

where $C_A$ is the parasitic capacitance associated with the node A. Consequently, decreasing the transconductance $g_m$ or bias current $I_b$ of the proposed auxiliary differential pairs M3 and M4 will inevitably introduce non-dominant doublets into the lower value to degrade the stability performance. Thus, the transconductances of the transistors M5 and M6 cannot be designed to be too small. To solve this issue, using short channel transistors can help mitigate the influence of these doublets by minimizing the parasitic capacitance. Compared with the conventional bulk transconductance double-enhanced input stage, the proposed technique in Fig. 3 improves the effective transconductance by $N$ times at no expense of additional current consumption.

As the improved effective transconductance, the input referred noise of the proposed bulk-driven input stage is decreased [23]. Neglecting the thermal noise contribution of the series gate and the bulk resistances, the expressions of the input referred thermal noise for the proposed bulk-driven input stage in Fig. 3 can be expressed as

$$V_{n,th}^2 \approx 2 \times 2nkT \times \frac{g_{m5}^2}{[(N+1)g_{mb}^2]} \times \left( \frac{g_{m5}}{g_{m5}^2} + \frac{1}{g_{m5}^2} + \frac{g_{m3}}{g_{m5}} + \frac{g_{m2}}{g_{m5}} \right)$$

(8)

From the above equations, the additional noise sources introduced by the auxiliary differential pairs are alleviated by the enhanced input transconductance to some extent. To minimize the thermal noise, one effective way is to increase the current consumption of the auxiliary amplifiers to achieve a higher value of $g_{m5}$.

2.4. The overall OTA with proposed input stage

The summing stage of the OTA uses the modified composite-transistor, which is shown in Fig. 4, to improve the dc gain of the OTA under low-voltage conditions [28]. The proposed structure consists of the series association of $M_a$ and $M_h$, which is composed of parallel association of unity transistors ($W/L_v$). The unity transistor connected to the drain terminal of the composite-transistor must be wider than connected to the source terminal ($N_h > N_v$), which forms T-type composite-transistor [29]. The overall OTA with the proposed input stage is shown in Fig. 5.

In the weak inversion region, the $V_{th}$ can be given by

$$V_{th} = \frac{kT}{q} \ln \left( \frac{N_b - W_u/L_u}{N_b - W_a/L_a} \right)$$

(9)

As above analysis, to saturate the transistor $M_a$, $V_{th}$ must be larger than $3kT/q$. Thus, the ratio $n$ of $N_b/N_v$ must be larger than 19.

Owing to the transistor $M_a$ of the composite-transistor is saturated, the overall output impedance of the modified compound–transistor pair can be given as

$$r_{out} = (g_{m,a}r_{in}) \cdot r_{in}$$

(10)

where $g_{m,a}$ and $r_{in}$ are the transconductance and the output impedance of unity transistor $M_a$. It is noticed that the output impedance of the modified composite-transistor is improved by a factor of $g_{m,a}$, which is almost 15–20 dB, when compared to single-transistor counterpart.

3. Simulation results and discussion

To compare the performance advantages of the proposed technique, we prototype three OTA versions: the first version is a OTA using the bulk-driven input stage (BD) as shown in Fig. 1; the second one is the OTA using the traditional double-enhanced bulk-driven input stage (DBD) as shown in Fig. 2; the third one using the proposed current–shunt auxiliary pairs bulk-driven input stage (EDBBD) as shown in Fig. 5. The summing stage of BD and BDBD is the same as that of proposed EDBBD and they are realized in a UMC 0.18 μm standard CMOS process, where the threshold voltages of NMOS and PMOS devices have relatively large values 0.4 V and 0.47 V, respectively. The performance metrics is obtained correspond to Spectre simulation tool and the MOS model is used the BSIM3v3. In this design, $N$ is chosen to be 3 according to previous analysis. Theoretically, the effective transconductance can be expected to be 4 times that of the conventional bulk-driven input stage. The biasing current of input pairs is 32 nA that of the auxiliary differential pairs is 12 nA and the power supply is 0.5 V which allows all the NMOS and PMOS transistors in the weak-inversion region, and load capacitance is 15 pF. The detailed aspect ratios of the proposed EDBBD OTA are given in Table 1.

Fig. 6 shows simulated AC response diagrams for three OTAs (BD, BDBD and EDBBD). The unity-gain bandwidth (GBP) of the BD, BDBD and EDBBD is 1.1 kHz, 1.88 kHz and 3.26 kHz respectively, which indeed demonstrates the enhanced transconductance of the proposed technique. Also, as discussed previously, as their output resistance does not depend on the output stage, hence any variation in the dc gain will be proportional to transconductance variation. Thus, the dc gain of the EDBBD OTA applying current–shunt auxiliary input stage is increased by a factor of 10 dB.

To study robustness to mismatch and process variations, Monte Carlo analysis with over 1000 runs was performed. The results are shown in Table 2. Note that there are a consistent 67.8 dB dc gain and 3.28 kHz in gain-bandwidth in using the proposed bulk-driven input stage with current–shunt auxiliary pairs, proving the feasibility of the proposed approach even under mismatches and process variations. Also, the results obtained for the phase margin demonstrate that the value selected for $N$ is not critical for circuit stability.

For the small signal transient analysis, shown in Fig. 7, a square wave of 50 mV is generated by a function generator at 0.5 kHz. Transient signals are measured with a voltage-follower configuration. The 1% rise settling times for the three OTAs are 0.21 ms, 0.3 ms and 0.64 ms respectively. Note that the EDBBD OTA with the proposed bulk-driven input stage has the shortest settling time.
which also demonstrates the enhanced transconductance of the proposed technique.

Table 1
Transistors aspect ratios of the proposed EDBD OTA.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W/L (μm/μm)</th>
<th>Transistors</th>
<th>W/L (μm/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1(2)</td>
<td>10/1</td>
<td>M3(4)</td>
<td>30/1</td>
</tr>
<tr>
<td>M5(6)</td>
<td>5/2</td>
<td>M7(8)</td>
<td>5/2</td>
</tr>
<tr>
<td>M9(10)</td>
<td>5/1</td>
<td>M11</td>
<td>120/1</td>
</tr>
<tr>
<td>M12</td>
<td>15/1</td>
<td>M13</td>
<td>10/1</td>
</tr>
<tr>
<td>M14</td>
<td>300/2</td>
<td>M15</td>
<td>5/2</td>
</tr>
<tr>
<td>M16(17)</td>
<td>5 × 2/1</td>
<td>M18(19)</td>
<td>100 × 2/1</td>
</tr>
<tr>
<td>M20(21)</td>
<td>2 × 2/1</td>
<td>M22(23)</td>
<td>40 × 2/1</td>
</tr>
</tbody>
</table>

Table 2
Simulated results from Monte Carlo analysis (1000 runs).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>EDBD OTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain average (dB)</td>
<td>67.8</td>
</tr>
<tr>
<td>DC gain standard deviation (dB)</td>
<td>0.9</td>
</tr>
<tr>
<td>GBW average (kHz)</td>
<td>3.28</td>
</tr>
<tr>
<td>GBW standard deviation (kHz)</td>
<td>0.14</td>
</tr>
<tr>
<td>Phase-margin average (°)</td>
<td>69</td>
</tr>
<tr>
<td>Phase-margin standard deviation (°)</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Fig. 5. The overall OTA with the proposed bulk-driven input stage.

Fig. 6. The simulated open-loop AC response of the three OTAs.

Fig. 7. The transient response of the three OTAs to square signal.

Fig. 8. The GBW of three OTAs versus input common-mode voltages.

Please cite this article as: X. Zhao, et al., Transconductance improvement method for low-voltage bulk-driven input stage, INTEGRATION, the VLSI journal (2014), http://dx.doi.org/10.1016/j.vlsi.2014.11.005
This demonstrates that the enhanced transconductance of the proposed EDBD OTA can be achieved at a rail-to-rail input voltage range. Fig. 9 shows the simulated input-referred noise of three OTAs. Note that the thermal noise of the BD, DBD and EDBD OTAs at 1 kHz is 840 nV/√Hz, 630 nV/√Hz and 560 nV/√Hz respectively. Hence, the noise performance of the EDBD OTA is better than the other OTAs (BD and DBD), which has been demonstrated by Eq. (8). This is attributable to higher dc gain of the proposed EDBD OTA caused by the enhanced effective transconductance in the proposed bulk-driven input stage. Large transistor dimensions are used in the weak inversion operation, in turn it minimizes the influence of noise, mainly the flicker noise that is dominant in a MOS transistor at low frequency.

Table 3 sums up a list of traditional BD OTA, the DBD OTA and the proposed EDBD OTA benchmark indicators used to evaluate this work. Also, the prior works compared to this paper are shown in Table 4. The figure-of-merit (FoM) is used for OTA performance comparisons and is expressed as

\[
\text{FoM} = 100 \times \frac{\text{GBW} \times C_L}{I}
\]

where \( I \) represents the current consumption of the OTA. This FoM is used to present the bandwidth and the drive capability of the OTA. According to these results, the EDBD OTA using the proposed current–shunt auxiliary bulk-driven input stage demonstrates the highest FoM. The proposed OTA design techniques are suitable for a wide range of low-voltage and low-power analog applications.

4. Conclusion

In this paper, a bulk-driven input stage with current–shunt auxiliary pair to significantly enhance transconductance is presented. The OTA using the proposed bulk-driven input stage is designed in a UMC 0.18 μm standard CMOS process. Due to the significant boost in the effective transconductance, the performance parameters of the proposed OTA such as unity-gain bandwidth and dc gain are all enhanced. Simulation results show that it has a higher FoM than traditional transconductance enhancement approach.

References


Huajun Fang was born in Heilongjiang province, China, in 1972. He obtained the M.Sc. degree from the Heilongjiang University, Haerbin, China and obtained the Ph.D. degree from the Tsinghua University (THU), Beijing, China. He has been with the Institute of Microelectronics of Tsinghua University (IMETHU), Beijing, China since 1999. Since 2009 he has been working as an Associate professor of the THU. His scientific interests are in the areas of integrated circuits and MEMS for integrated microsystem.

Xiao Zhao was born in Shandong province, China, in 1985. He received the M.Sc. degree in electrical engineering from the Beihang University, Beijing, China, in 2009. In 2013, he received Ph.D. degree in microelectronics from Tsinghua University, China. He is currently teaching in School of Geophysics and Information Technology, China University of Geosciences, Beijing, China. His research interests include mixed-signal integrated circuits, high performance OTA and high precision data-converters.

Tong Ling was born in Hunan province, China, in 1989. He received the B.Sc. degree in automation from the Changsha University of Science & Technology, Changsha, China, in 2012. He is currently pursuing the M.Sc. degree at the Institute of Microelectronics, Tsinghua University, Beijing, China. His research activities are focused on high precision operational amplifiers and data-converters.

Jun Xu was born in Anhui province, China, in 1963. He obtained the M.Sc. degree and the Ph.D. degree from the 77th Research Institutes of Ministry of Aeronautics Industry, Beijing, China. He has been with the Institute of Microelectronics of Tsinghua University (IMETHU), Beijing, China since 1994. Since 1997 he has been working as an Associate professor of the THU. And now he is the professor of the THU. His scientific interests are in the areas of integrated circuits and industrial test facilities.